

In the Response to Arguments, the Examiner stated that the "Yeh reference discloses in Fig. 3, VWL is connected to the gates 38 and 44 (see column 11 and 12, equations 1 and 2, where the VWL could be equal to VFG); and VWL is a control potential, or a word line (column, the last line)." Applicant does not agree with this statement. As shown in Figs. 3 and 4 of Yeh, a tunneling element 30 exists between the control potential VWL and the floating gate potential VFG. While it is true that VWL and VFG could be the same potential, it is improper to assert that VWL is a word line commonly connected to the gates of transistors 38 and 44. In fact, VWL is not connected to the gate of the transistor 44. Accordingly, Applicant submits that Yeh clearly fails to disclose or suggest a word line coupled to the gate of the depletion mode transistor and the gate of the enhancement mode transistor.

Yeh further fails to disclose or suggest the cell plate of the claimed invention. According to the claimed invention, a first terminal of the ferroelectric capacitor is coupled to a drain of the enhancement mode transistor and a second terminal of the ferroelectric capacitor is coupled to a cell plate. In contrast, according to Yeh, one terminal of a capacitor Cs is coupled to a drain of a floating gate transistor and the other terminal of the capacitor Cs is connected to the floating gate 50, which is clearly not a cell plate.

Moreover, as well known to a person having ordinary skill in the art, the claimed invention is directed to a random access memory device while Yeh is directed to a non-volatile integrated circuit memory device. In other words, the mechanisms of these two devices are distinctively different. That is, the ferroelectric capacitor of the RAM device has been used to store data in the claimed invention, whereas a floating gate of the non-volatile integrated memory device has been used to store data, according to Yeh. Because of this difference, one terminal of the capacitor is coupled to a drain of the enhancement mode transistor and the other terminal is coupled to a cell plate, according to the claimed invention. To the contrary, one terminal of the capacitor Cs is using an active area and the other terminal of the capacitor Cs is coupled to a floating gate. Accordingly, Yeh clearly fails to disclose or suggest the ferroelectric capacitor of claim 1.

For all of the reasons discussed above, claim 1 and its dependent claim 4 are not made obvious over Yeh in view of Hayt under 35 U.S.C. §103(a).

Claims 2, 3, 5-8 and 9 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Yeh in view of Hayt, and further in view of Hoffman. Applicant traverses the rejection for the following reasons.

As set forth above, claim 1 is patentable over Yeh in view of Hayt under 35 U.S.C. §103(a), and Hoffman does not supply the

above-noted deficiencies of Yeh and Hayt. Therefore, claims 2 and 3, which are dependent on claim 1, are patentable for the reasons discussed above with respect to claim 1, as well as on their own merits.

Applicant submits that claim 5 is directed to a ferroelectric random access memory device including a plurality of ferroelectric memory cells. In addition to the reasons set forth above with respect to claim 1, Yeh further fails to disclose or suggest the plurality of ferroelectric memory cells. As set forth above, Yeh and Hayt, either alone or in combination, fail to disclose or suggest all of the features of claim 1, and Hoffman does not supply the above-noted deficiencies of Yeh and Hayt. Therefore, claim 5 and its dependent claims 6-9 are patentable for the reasons discussed above with respect to claim 1, as well as on their own additional merits.

All objections and rejections having been addressed, it is respectfully submitted that claims 1-9 are now in condition for allowance and a notice to that effect is earnestly solicited. If any issues remain to be resolved, the Examiner is cordially invited to telephone the undersigned attorney at the number listed below.

Respectfully submitted,

By:  _____

Yoon S. Ham
Reg. No. 45,307
Direct Tel.: (202) 662-8483

JACOBSON HOLMAN, PLLC
The Jenifer Building
400 Seventh Street, N.W.
Washington, D.C. 20004-2201
(202) 638-6666

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